Module 6: Building the Project

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Module Seq = 6

6.1 Assigning designators

The Schematic Editor includes a positional-based re-annotation tool for allocating component designators.

6.1.1 Using Annotate to assign designators

The Schematic Editor provides an automated method of assigning designators. This is the Annotate command. This will take any component which has '?' appended to its designator and allocates a unique designator to those parts.

The order in which designators are assigned is based on the components' position on the sheet. The *Annotate* dialog allows you to set one of four positional annotation options. The annotation grid is based on the sheet border reference, so change the number of regions in the border reference to control the annotation grid.

To run Annotate, choose the **Tools » Annotate Schematic** menu command. This displays the *Annotate* dialog shown in Figure 1.

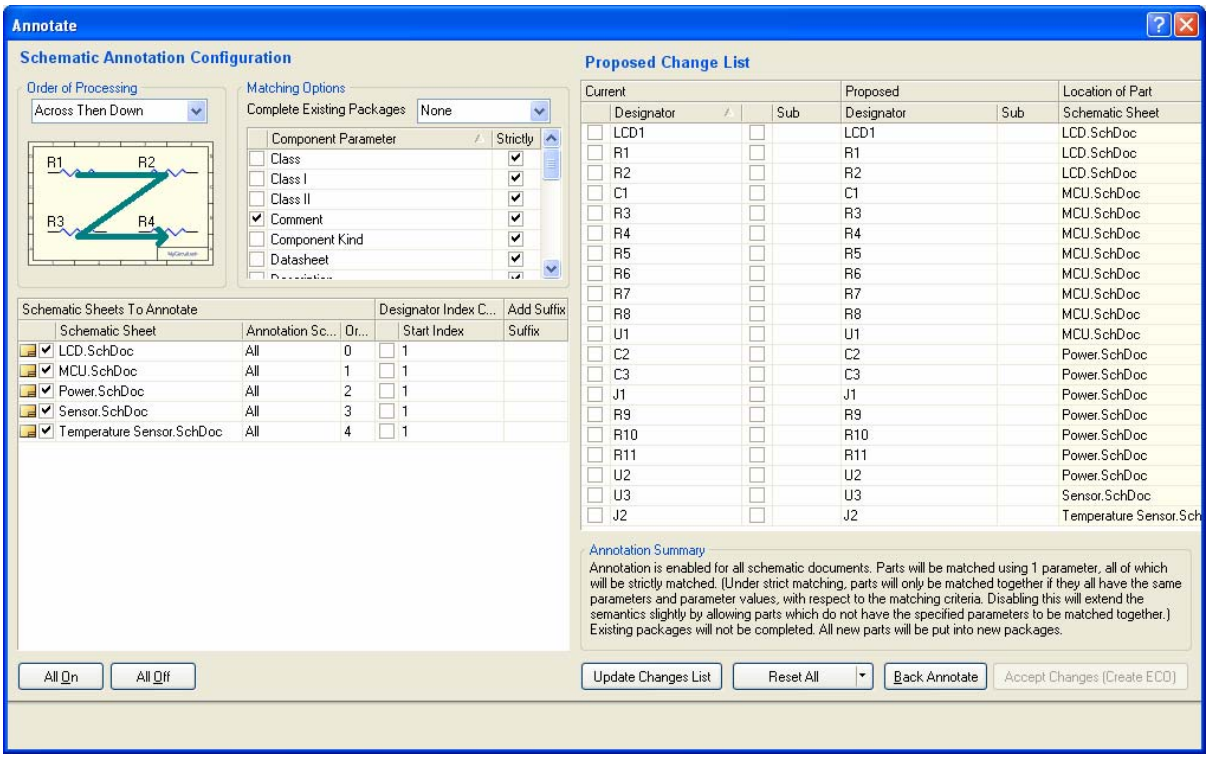

Figure 1. Annotate dialog

The Annotate options include:

- **Update Change List –** this button will reassign all designators that are not currently assigned (their designator currently ends in a ?).
- **Reset All –** use the Reset All button to reset all designators so that they end in a ?. You can also limit this to resetting only duplicates.
- **Order of Processing –** there are four directional options available. Select the preferred one at the top left of the dialog. This uses the sheet grid to define the across/down increments.
- **Matching Options –** enable the parameters to be used to package parts of a multi-part component. Typically, this is based on the component comment. If there are particular parts that must be packaged together, give both a common parameter and enable this parameter

in the **Component Parameter** list (e.g. filter-stage1). Note that the **Annotation Summary** down the bottom right of the dialog gives information about the matching behavior.

- **Schematic Sheets to Annotate –** this section of the dialog gives sheet-by-sheet control of the annotation, sheets can be excluded from the process and you can also control the annotation starting number for each sheet.
- **Back annotate –** click this to load a Was/Is file. This is only required if the board is not being designed in Altium Designer. If you are designing the board in Altium Designer you can back annotate directly from the PCB to the schematic by selecting the **Design » Update** menu option.
- Whenever an **Update** or **Reset** is performed an *Information* dialog will appear. This dialog details how many changes have been made from the previous state (since the last Update or Reset) and the information *dialog* also lists the changes from the original state (since the *Annotate* dialog was opened).
- Once you are happy with the designator assignments, click the **Accept Changes** button to generate an ECO. From the *ECO* dialog you can update the schematic.

Note: To prevent a component from having its designator changed by the Annotation process, enable the **Locked** checkbox adjacent to the **Designator** in that component's *Component Properties* dialog.

6.1.2 Designators on multi-part components

The suffix for multi-part components can be either Alpha or Numeric, depending on the Alpha Numeric Suffix option in the *Preferences* dialog. This is an environment setting and will apply to all open schematic sheets.

You can change parts within a component using the **Edit » Increment Part Number** command. Select this command and then click on the part of interest.

Note: To prevent multi-part component parts being swapped during the annotation process enable the **Locked** checkbox adjacent to the Part selector in the *Component Properties* dialog.

6.1.3 Project Order

The project order of a project is the order the documents appear in the projects panel. However when dealing with hierarchical designs, due to the top sheet becoming the root schematic, the project order can be difficult to determine. To make this process easier an option in the preferences can be turned on to see the project order numbered position. To turn this on goto **DXP » Preferences » System » Projects Panel**. In the General category, tick on the option **Show document Position in project**. Click **OK**, once ticked.

The picture in Figure 2 shows the numbering that appears when the position is shown. Once this data appears, the order can be changed by dragging and dropping the documents in the project panel to change the project order.

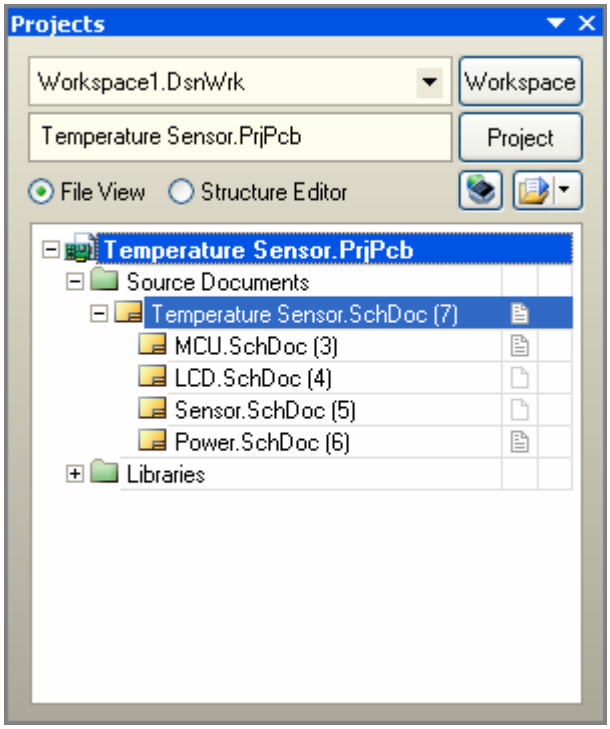

Figure 2. Project panel with project order showing

6.1.4 Exercise – Annotating the design

1. Select **Tools » Annotate Schematics** from the menus.
2. In the *Annotate* dialog, click the **Reset All** button, then click **OK** in the *Information* dialog that appears. Note that the **Proposed Designator** column in the dialog now shows all designators having a ? as their annotation index.
3. The Order the schematics will be annotated is configured in the **Schematic Sheets to Annotate** section of the dialog. You can change the Order manually, or you can right click and select **Order Alphabetically** or **Order By Project Order**, as shown in Figure 3. To check each schematic's position in the project order, enable the **Show Document Order** in Project option in the **System – Project Panel** page of the *Preferences* dialog and the number will be displayed in the Projects panel.

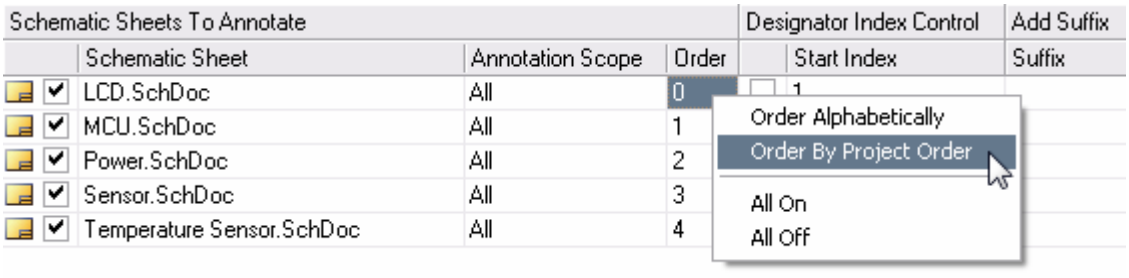

Figure 3. Setting the sheet numbering order to Order By Project Order.

4. Altium Designer supports annotating each sheet from a fixed starting index, to use this feature tick all the **Designator Index Control tick** boxes, as shown in Figure 4.

Schematic Sheets To Annotate				Designator Index Control	Add Suffix
	Schematic Sheet	Annotation Scope	Order	Start Index	Suffix
☑	Temperature Sensor.SchDoc	All	0	☑ 100	
☑	MCU.SchDoc	All	1	☑ 200	
☑	LCD.SchDoc	All	2	☑ 300	
☑	Sensor.SchDoc	All	3	☑ 400	
☑	Power.SchDoc	All	4	☑ 500	

Figure 4. Set the Starting Index for each sheet

5. Now set the **Start Index** for each sheet, as shown in Figure 4.
6. Click the **Update Changes List** button to assign a unique designator to each component. The components are annotated positionally, according to the direction setting selected at the top left of the **Annotate** dialog. The *Information* dialog that appears indicates how many designators have changed from their original state.
7. Repeat the process of resetting and assigning, trying different direction options (the actual designators on the schematic are not being changed as you do this). Finish with a direction option that you prefer.
8. To commit the changes and update the components, click the **Accept Changes** button to generate an ECO. Click **Execute Changes** in the *ECO* dialog, then close the *ECO* and the *Annotate* dialogs.

Note: Changes are only made if the ECO is executed.

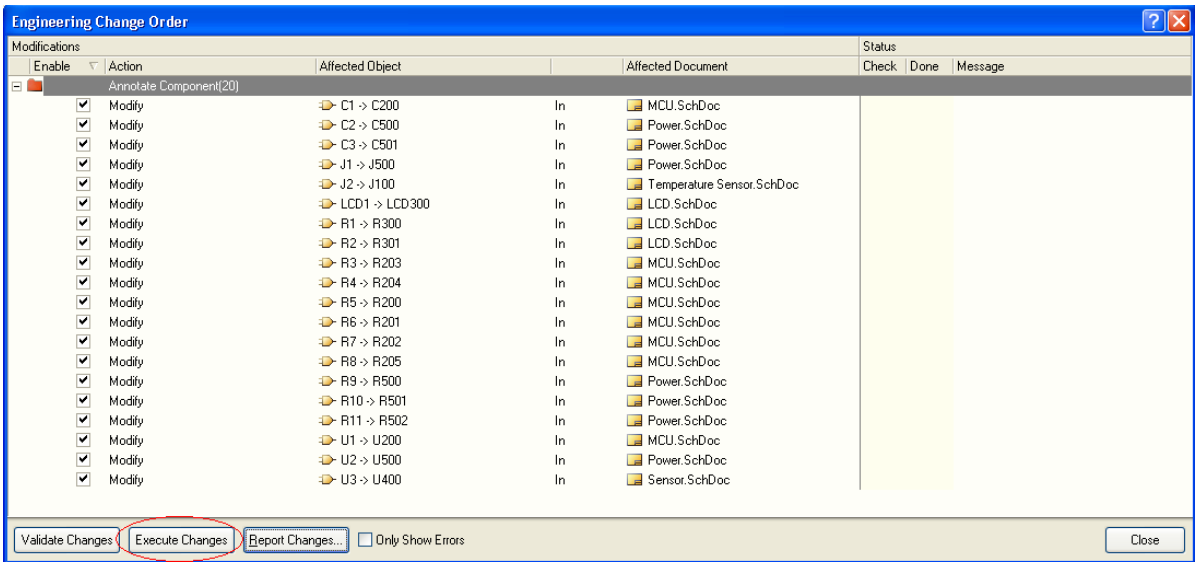

Figure 5. Engineering change order dialog for annotation changes,

9. Note that each document that has been affected by the changes has an * next to its name on the document tab at the top of the window. Save all documents in the project.

6.2 Compiling and verifying the project

This section looks at how to verify a design, an essential step before transferring to PCB layout. In Altium Designer, checking the design is done by *compiling* the design which checks for logical, electrical and drawing errors.

To compile your design, select **Project » Compile PCB Project** or use the **CC** shortcut.

Compiled results are displayed in the **Messages** panel; from here, you can double-click to jump to an error or warning. The **Messages** panel will only open automatically if there are errors, if it is not visible click on the **System » Messages** button at the bottom of the workspace to display the panel.

Note: The default error checking options are on the cautious side, you should always review the settings in the *Project Options* dialog and adjust them to suit your project and design requirements.

Once the design has been compiled, it can be navigated in the **Navigator** panel.

6.2.1 Setting up to compile the design

When you compile the design, DXP builds a connective model of the design – you can think of it as an internal netlist. The presence of the internal netlist allows you to navigate or browse the connective structure of the design.

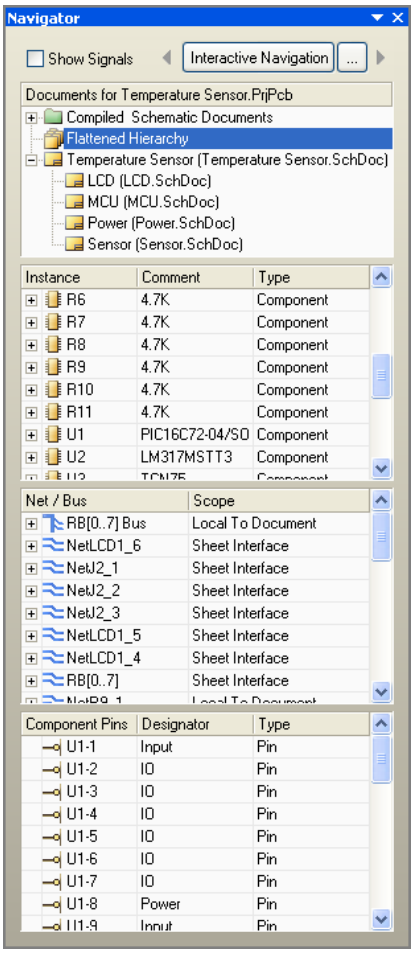

Figure 6. Use the Navigator to check the design connectivity

6.2.1.1 Compiler options

- Before the design can be compiled, the project options must be configured. This is done in **Options** tab of the *Options for Project* dialog (**Project » Project Options**).
- The **Net Identifier Scope** must be appropriate for the structure of the design. This was covered in *Module 5 - Multi-Sheet Design*.
- When the design is compiled, it can be navigated using the Navigator panel. The Navigator can be brought up by going to the panel control in the bottom right and selecting **Design Compiler » Navigator**. Select the **Flattened Hierarchy** at the top of the **Navigator**. When you click on a component or a net, that component or net will be displayed in the workspace.
- Expand the component or net using the small + sign to access all pins in the component or all pins/net identifiers in the net.
- Click the ... button to the right of the Interactive Navigation button to configure options that control how the workspace will be displayed.
  - **Zoom:** jump to the sheet and zoom in on the object of interest.
  - **Select:** select the objects of interest.
  - **Mask:** fade all objects except those of interest. Control the mask fade level using the **Mask Level** button at the lower right of the screen. Clear the Mask using the **Shift+C** shortcut.

- **Connective Graph:** show the connective relationship with either red (for net objects) or green (components) graph lines.

- The Navigate button in the panel allows you to navigate spatially. Click it to get a crosshair cursor, then click on an electrical object in the workspace, such as a wire, net label, port etc, to highlight all electrical connected objects.
- To move Up/Down in the hierarchy hold down the **CTRL** key and double click on either a sheet entry, Sheet symbol or Port to navigate the design.

6.2.1.2 Error Reporting options

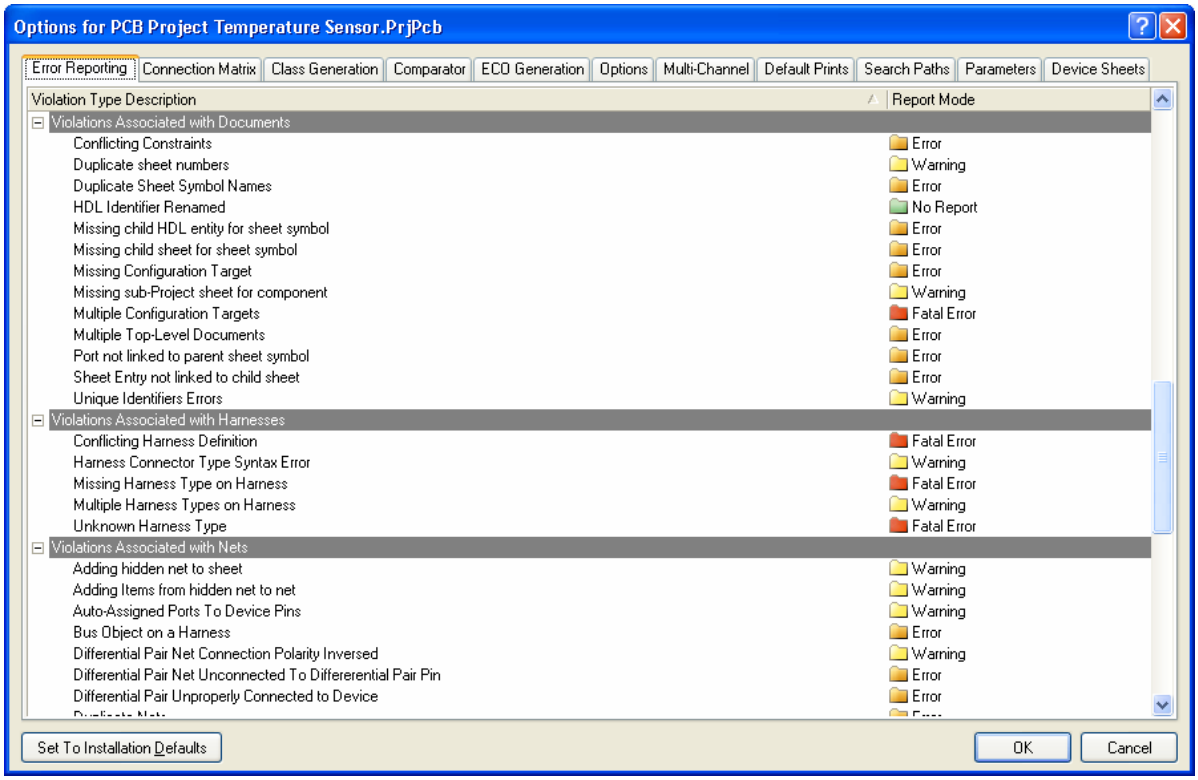

Figure 7. Setup for Error Reporting

- Error reporting options are configured in the **Error Reporting** tab and the **Connection Matrix** tab.
- There is an extensive array of error reporting options which have default settings that are on the cautious side. Generally, it is better to compile the design and then if there are warnings that are not an issue for your design, change the reporting level.
- One option of interest is **Nets with only one pin**. This can be used to find single node nets, where a pin has been connected to a port or Netlabel, but does not connect to another pin. This is set to **No Report** by default.

6.2.1.3 Connection Matrix

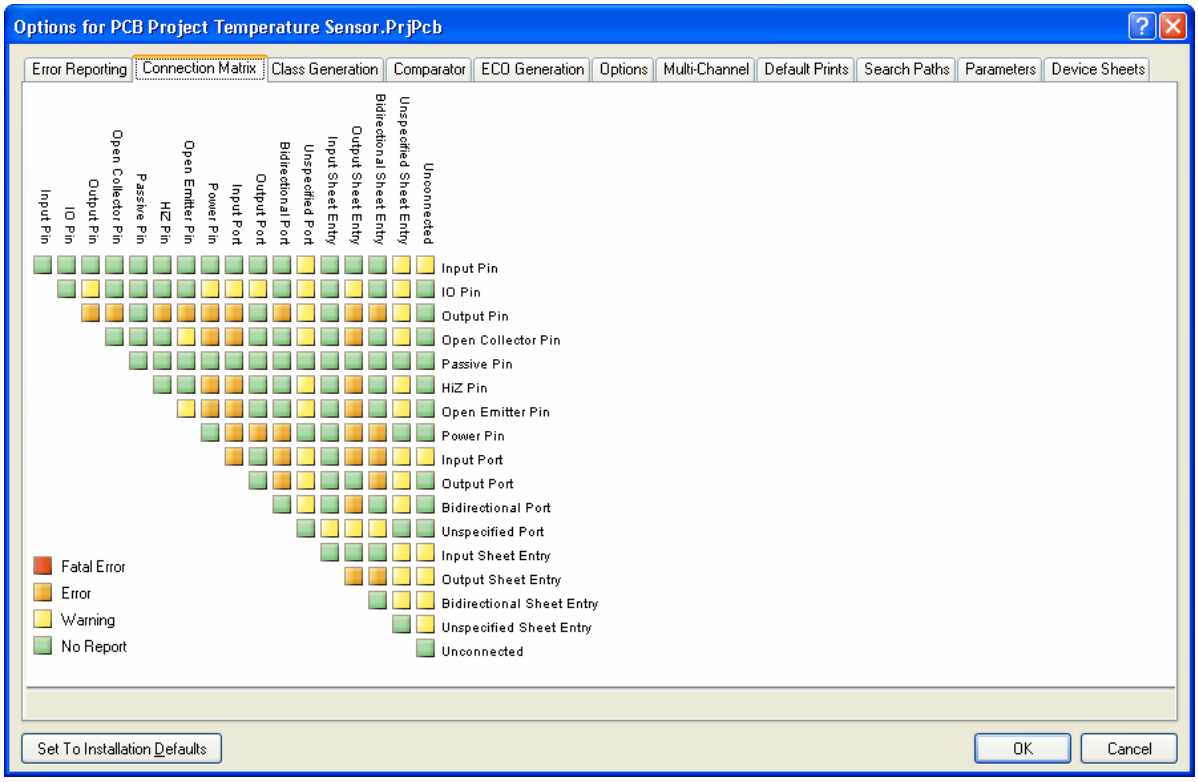

Figure 8. ERC Rule Matrix tab

- The **Connection Matrix** tab in the *Options for Project* dialog is shown in Figure 8. This matrix provides a mechanism to establish connectivity rules between component pins and net identifiers. It defines the logical or electrical conditions that are reported as warnings or errors.
- For example, an input pin connected to an input pin would not normally be regarded as an error condition, but connected output pins would not. This is reflected in the table.
- Rules can be changed by clicking on the appropriate square in the matrix, causing it to cycle through the available options.

6.2.2 Interpreting the messages and locating the errors

- When you compile the project, any conditions which generate a warning or error will be listed in the **Messages** panel. Note that the **Messages** panel will only open automatically if there is an error condition.
- Double-click on a warning/error to pop up the **Compile Errors** panel, then double-click on an object in that list to jump to it on the schematic.
- Right-click in the **Messages** panel to clear messages. Click on the column headings to sort by that column. Double-click on a message to display the **Compile Errors** panel in which you can double-click to cross probe to that object.
- Subsequent compilations will remove warning/error messages once the error conditions have been corrected.
- It is important to examine each warning/error and resolve them, change the error checking Report Mode, or mark them with a No ERC marker. This should always be done prior to transferring the design to PCB layout.

6.2.2.1 Exercise – Configuring the project options

1. Select **Project » Project Options** to display the *Options for Project* dialog and click on the **Options** tab.
2. For this project, the **Net Identifier Scope** can be left on automatic. Enable only the **Allow Ports to Name Nets** in the **Netlist Options**.
3. Click **OK** to save the settings. Note that the Project PCB file has been modified. You should save the Project PCB file.

6.2.2.2 Exercise – Design verification

1. Check your design by compiling your design and checking any errors or warnings.
2. Resolve any errors. Note that **Nets with no driving source** reports any net that does not contain at least one pin of the following electrical types: IO, Output, OpenCollector, HiZ, Emitter or Power.
3. If you have any remaining warnings that will not affect your design, you can consider turning that warning type to *No Report* in the **Error Reporting** tab of the *Options for Project* dialog.

Some tips

- Examine each of the objects associated with the error.
- Enable the Graph option to examine the connectivity of a net. Once a net is selected in the Navigator panel, it is highlighted throughout the design. You can also ALT+click on a net to highlight it on the current sheet.
- Errors with input pins are often due to problems with their source. If the input looks OK, trace the signal back to the source (output pin / port).

Note: To open a sub-sheet, hold CTRL as you double-click on the sheet symbol.