Neural Network with MIN/MAX Nodes for Image Recognition and Its Implementation in Programmable Logic Devices

Radek Holota
Information and Electronic Technologies
New Technologies Research Centre
Univerzitni 8, 306 14 Pilsen
Czech Republic
radek.holota@centrum.cz

***Abstract* – This article deals with a method of image recognition based on neural networks composed of MIN/MAX nodes. The general concepts of the MIN/MAX nodes and the neural networks are outlined. The developed software system is then briefly introduced. Finally, the design of the neural networks in VHDL (VHSIC Hardware Description Language) is presented.**

I. INTRODUCTION

At present there is a large development of the image recognition systems. One of the possibilities is utilization of neural nets. This possibility has been the main subject of cooperation between the Dept. of Applied Electronics, University of West Bohemia and the Dept. of Electrical and Electronic Engineering (now Electronic and Computer Engineering) at Brunel University over the past decade.

This cooperation has been mainly focused on the neural nets with n-tuple nodes [1] and MIN/MAX nodes [2,3]. The network of MIN/MAX nodes could respond directly to multi-level values and so it could provide powerful pattern recognition properties. The natural progression of this technique was to consider the recognition of coloured images and the feasibility of such a system was later proposed [4,5]. In spring 2000 a software system [6,7] was designed which implements both methods – n-tuple and MIN/MAX and image pre-processing part [8]. This work was done under auspices of the Erasmus Student Exchange Scheme.

At present a hardware system is being developed in New Technologies Research Centre. This system implements single layer network based on MIN/MAX nodes [9] in programmable logic devices esp. Field Programmable Gate Arrays (FPGAs).

II. BACKGROUND

The MIN/MAX node technique may be considered similar to template matching, which measures the nearest distance of the test pattern to stored reference patterns. However, unlike template matching, for MIN/MAX nodes, no distance measure calculations are required as each MIN/MAX node operates as a simple 'look up table' and thereby enables fast operational speeds. Also, several training images can be stored within each net and thereby provide several patterns per class.

A. MIN/MAX node

The neural networks are composed of high amount of executive units – neurons. In this case the executive unit is MIN/MAX node Fig. 1. In principle, for the relevant class,

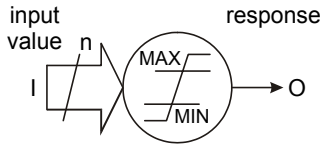

Fig. 1. MIN/MAX node

each node stores the absolute Minimum and Maximum (MIN/MAX) values, which occur during training. On classification, each node will then respond with a '1' to any level between, and including, the 'MIN/MAX' values, which were stored during training. In order to improve generalisation, offsets, greater than the maximum value and less than the minimum value, may be added, or subtracted, to allow for noise, illumination, translational and rotational variations not included in the training set.

Mathematical description:

$$O = F(I), \tag{1}$$

$$F(x) = \begin{cases} 0 \ldots x \in (0, MIN) \cup (MAX, 2^n - 1) \\ 1 \ldots x \in \langle MIN, MAX \rangle \end{cases}, \tag{2}$$

where I is n-bits input value of MIN/MAX node and so $I \in \langle 0, 2^n\text{-}1 \rangle$. $F(x)$ is transfer function of the node and is defined as (2). O is response of the node. And value MIN (MAX) is the absolute minimum (maximum) value which occurs during training.

B. Single Layer Network (SLN)

There are many different types of the neural networks (different structures, number of layers, using feedback or not, etc.). For our purposes a single layer network with

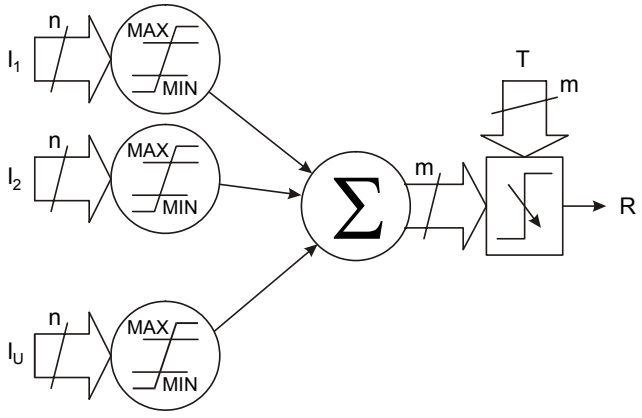

Fig. 2. Single Layer Network

structure shown in Fig. 2 was used. This network is composed of one layer of the MIN/MAX nodes. Their responses are added together by summation unit. This response is finally tresholded by a preset value. So the final response of this network is 1 (for similar images) or 0 (for different images).

Mathematical description:

$$R = G\left(\sum_{i=1}^{U} F(I_i)\right), \tag{3}$$

$$G(x)\begin{cases} 0 \ldots x < T \\ 1 \ldots x \geq T \end{cases}, \tag{4}$$

where I is n-bits input value of MIN/MAX node and so $I \in \langle 0, 2^n\text{-}1 \rangle$. $F(x)$ is transfer function of the node and is defined as (2). U is the number of nodes in the network. The function $G(x)$ realizes a threshold with preset m-bits value T, where $m \geq log_2 U$, and R is final response of the network.

C. Utilisation in colour image recognition

Main advantage of the MIN/MAX nodes is that they could respond directly to multi-level value. So the neural network with MIN/MAX nodes can be used directly in greyscale image recognition. For colour image recognition, a 'trixel' MIN/MAX node shown in Fig. 3 has to be implemented. The 'trixel' MIN/MAX node is composed of three MIN/MAX nodes, each for one colour component and a logical AND which generates the final response of the node. The number of 'trixel' nodes is equal to the number of pixels which are used for training from the input pattern. The number can be reduced for higher processing speed. Coverage about 10% is usually enough for recognition. Then the pixels are pseudo-randomly mapped from the input pattern. Several techniques can be used for improving the response. It is possible to add tolerance band for MIN/MAX nodes which allow small changes in illumination. And the grouping technique improves the differences between responses to a right image and different images.

Fig. 4 shows the neural network based on 'trixel' MIN/MAX nodes where the grouping technique is applied. The pixels are pseudo-randomly mapped from the input

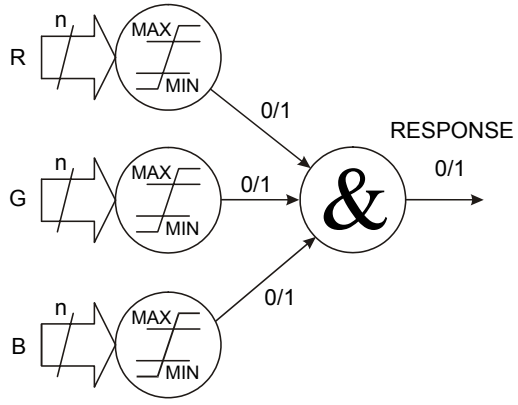

Fig. 3. 'trixel' MIN/MAX node

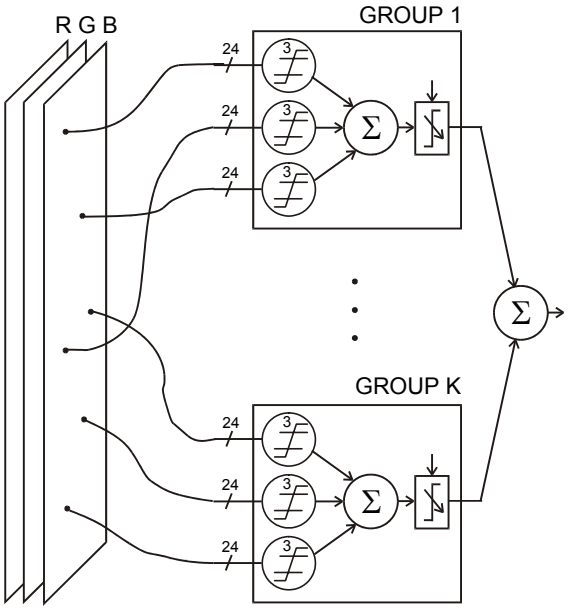

Fig. 4. Neural network with 'trixel' MIN/MAX nodes and grouping for colour image recognition

pattern (in RGB colour space) and fed to grouped 'trixel' MIN/MAX nodes. The responses are summed and thresholded in each group. The final response is the summation of responses of all groups.

III. SOFTWARE SYSTEM "WISARD II"

As mentioned above, the software system named WISARD II was designed in cooperation between Brunel University and University of West Bohemia. This system can be used for testing of colour image recognition based on neural networks or non-real-time application of colour image recognition. This software is mentioned here because it is a powerful tool in the testing of the properties of neural network with MIN/MAX nodes and the possibilities of utilisation in image recognition.

The software system consists of two main parts. The first part implements image pre-processing techniques, esp. position, rotation and size normalisation. The second part implements image recognition techniques based on neural network with n-tuple and MIN/MAX nodes. Both mentioned improving techniques (tolerance band, grouping) are fully implemented in the software system. So this software is powerful tool for tuning the best parameters for future hardware system.

IV. NEURAL NETWORK UNIT IN VHDL

At present a simple unit in VHDL is developed for the realisation of neural network by programmable logic devices. The first decision during the design was how to make the memory for storing absolute minimum and maximum value of the MIN/MAX nodes. There are several possibilities. The memory can be implemented by using direct logic cells, embedded memory blocks or external memories. In our case, the development board with device FLEX10K20 (FPGA Altera) [10] was used. This device has six Embedded Array Blocks (EABs). It was possible to use these blocks because only small neural network has been designed. It is necessary to use external memories for large neural networks.

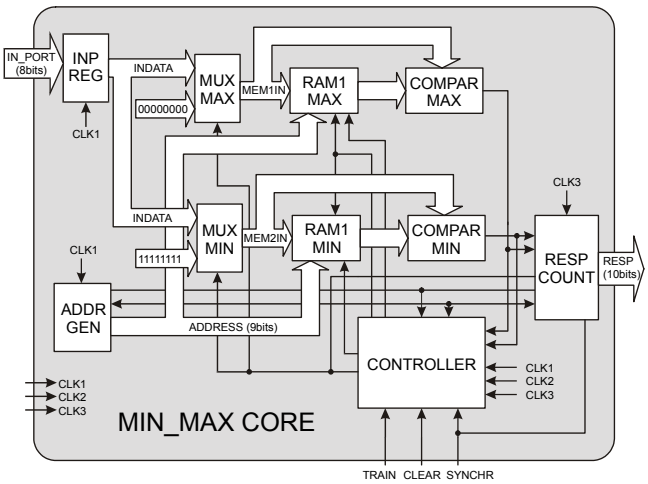

Fig. 5. Block scheme of the designed system

The design process started with the design of a system structure. This structure is shown in Fig. 5. The whole system consists of partial blocks. These partial blocks are simple in our case and they are described directly in VHDL. For the description of memories for storing minimum and maximum values a block from Library of Parameterised Modules (LPM) is used.

The designed block in VHDL realises the neural network which corresponds with Fig. 2 with one exception. The threshold of response is not included. The response of block is only summed responses of nodes. The depth of input values is *n=8 bits*, the number of nodes is *U=512* and the depth of response is *m=10 bits*. An interface of the block is composed of following signals and buses. *IN_PORT* is 8 bits input bus. The signal *TRAIN* determines the phase of processing (train/recognise). The signal *CLEAR* is for the initialisation of memories. The signal *SYNCHR* synchronises reading. There are three clocking signals *CLK1*, *CLK2* and *CLK3*. A stand-alone block serves these clocking signals. The output of the block is 10-bits bus named *RESPONSE*.

A block diagram of designed system is shown in Fig. 5. The input values are captured in the input register (*INP REG*). The capture value is fed to the multiplexers (*MUX MAX* and *MUX MIN*). These multiplexers switch between the captured value (for training/recognition) and values "*00000000*" or "*11111111*" (for initialisation of memory). The comparators (*COMPAR MAX* and *COMPAR MIN*) compare the input value with the stored value in the memories (*RAM1 MAX* and *RAM2 MIN*) at the address generated by the address generator (*ADDR GEN*). In accordance with the result of comparing is or isn't incremented the response counter (*RESP COUNT*), and the signals generated for writing to the memories during a training phase. The control unit (*CONTROLLER*) controls all units of the system and their cooperation.

IV. CONCLUSION

The main goal of this work was to outline the possibilities of utilisation of neural networks in image recognition. The article is mainly focused to the networks based on MIN/MAX nodes and 'trixel' MIN/MAX nodes (for colour image recognition). A part of this work is the design of a system which implements single layer network in FPGAs. Whole description of the system is in VHDL. The designed block in VHDL can be utilised in the design of more complex image recognition systems or another systems based on neural network with MIN/MAX nodes.

V. ACKNOWLEDGMENT

This paper is based upon work sponsored by the Ministry of Education of the Czech Republic under research and development project LN00B084.

VI. REFERENCES

[1] V. Georgiev and B. A. Wilkie, "Colour Recognition using the n-tuple methodology," in *Proceedings of the International Symposium "Applied Electronics 1995",* University of West Bohemia, Pilsen, pp. 97-102.

[2] R. J. Ollier, *"Grey Scale Template Matching System (GSTMS),"* B.Eng. final year report, Dept. of E.E.&E., Brunel University, April 1994.

[3] B. A. Wilkie, "The use of arrays of grouped 'MAX/MIN' nodes as an aid to pattern recognition," in *Proceedings of the International Conference "Applied Electronics '98'"*, University of West Bohemia, Pilsen, pp. 214-218, ISBN 80-7082-443-3.

[4] B. A. Wilkie, "A proposed colour recognition system utilising networks of grouped 'MIN/MAX' nodes," in *Proceedings of the International Conference "Applied Electronics '99'"*, University of West Bohemia, Pilsen, pp. 211-219, ISBN 80-7082-512-X.

[5] B. A. Wilkie, R. Holota, J. Fiřt "A colour image recognition system utilising networks of trixel n-tuple and MIN/MAX nodes," in *Proceedings of the International Conference "Applied Electronics 2001"*, University of West Bohemia, Pilsen, pp. 262-269, ISBN 80-7082-758-0.

[6] J. Trejbal, *"Software realisation of a colour image recognition system using n-tuple and MIN/MAX node neural networks,"* Diploma project report, Dept. of Applied Sciences, University of West Bohemia, May 2000.

[7] R. Holota, J. Trejbal, B. A. Wilkie, "Software realisation of a colour image recognition system with an image normalisation stage," *Proceedings of the University of West Bohemia*, section 1, vol.4/2000, pp. 75-86, ISBN 80-7082-718-1, ISSN 1211-9652.

[8] R. Holota, *"Position, size and rotation normalisation,"* Diploma project report, Dept. of Electrical Engineering, University of West Bohemia, May 2000.

[9] R. Holota, "Návrh makra neuronové sítě v jazyce VHDL," *Elektrorevue* [online], vol.46/2001, URL: http://www.elektrorevue.cz/clanky/01046/. ISSN 1213-1539.

[10] Altera, *Device Data Book 1999*, May 1999, p.1035.