Digital signal generator for railway signalling technology

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Abstract: - This article deals with a design of a digital signal generator for the railway signalling technology. At present time signal generators and phase sensitive receivers are used as the railway signalling technology by the Czech Railways. These signal generators and phase sensitive receivers are used for detecting the presence of railway vehicles at the rail circuit and for checking of the rails integrity. The digital signal generator was designed using a direct digital synthesis. The generator is realized by VHDL language and implemented in a FPGA (Field Programmable Gate Array) device.

Key-Words: - signal generator, direct digital synthesizer, phase sensitive receiver, railway signalling technology

1 Introduction

At present time signal generators and phase sensitive receivers are used as the railway signalling technology by the Czech Railways. These signal generators and phase sensitive receivers are used for detecting the presence of railway vehicles at the rail circuit and to check the integrity of the rails.

The railway circuit is shown in Figure 1. The railway circuit consists of an isolated rail segment, transformers, the signal supply (*SS*) and the phase sensitive receiver (*PSR*).

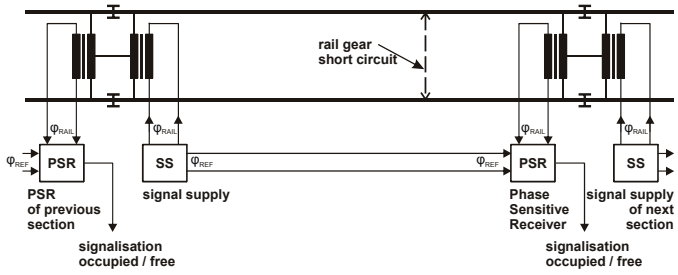

Fig. 1 Railway circuit

The signal supply is source of the signalling frequency. The signal supply generates the 75 Hz or 275 Hz sinusoidal signal. The signal supply have two phase shifted outputs (frequently is used phase shift equal to 90 degrees). One of the outputs is connected through the transformer to the beginning of railway segment. The second output is connected to the reference input of the phase sensitive receiver. At the opposite end of the railway segment is signal from the second transformer connected to the second input of the phase sensitive receiver. The presence of the railway vehicle in the railway segment can be detected by changes in the amplitude and phase of the rail signal compared to the reference signal. The change of both the amplitude and phase is detected by the phase sensitive receiver. There are exist two groups of phase sensitive receivers: electro-mechanic and electronics receivers.

1.1 Phase sensitive receivers

The electro-mechanic phase sensitive receiver is based on a two-phase inductive relay (phase sensitive relay). The phase sensitive relay is working on the principle well known as Ferraris motor. The phase sensitive relay consists of two coils turned over 90 degrees. Between the coils is inserted plate made from conductive non-ferromagnetic material (aluminium plate). This aluminium plate then acts by torque M on contacts. The torque M is proportional to the product of currents in coils and function $\sin\varphi$ (Equation 1).

$$M \approx kI_1 I_2 \sin\varphi \tag{1}$$

Where the φ is phase angle between currents I_1 and I_2. From Equation 1 is evident that the maximum moment happens when the phase angle φ is equal to 90 degrees.

The electronic phase sensitive receivers measure and compare the amplitude and the phase of the rail signal and compare it against reference signal [4]. The electronic phase sensitive receivers have advantage of adjustable phase shift and better immunity to interfering currents.

2 Signal supply

A block diagram of the signal supply is shown in Figure 2. The signal supply consists of a power circuit (*PWR*), a signal generator (*SG*), power amplifiers (*PA*), a supervising circuit (*SC*) and output transformers (*OTr*).

The signal generator generates two phase shifted square wave signals which are amplified by amplifiers and transformed by output transformers. The phase shift between outputs is adjustable in the range of 0 to 180 degrees with 15 degrees step. The output voltage of signal supply is the square wave signal with an effective value of the fundamental harmonic 220V. The signal source can work independently or synchronized from an external source.

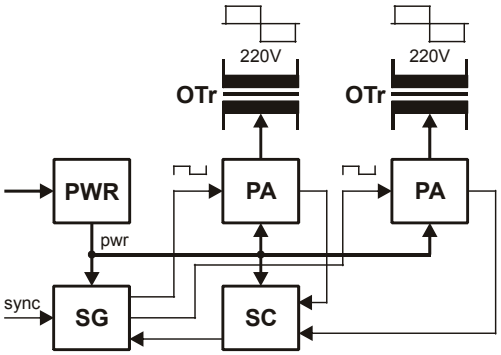

Fig 2. Block diagram of signal supply

The disadvantage of this supply is that it generates the square wave output signals, which cause variety of harmonic frequencies at the output signal. To obtain pure sine wave outputs we started to design new digital signal generator.

The aim was to change the signal supply block by changing the signal generator module (*SG*) only. The block diagram of improved signal supply is shown in Figure 3.

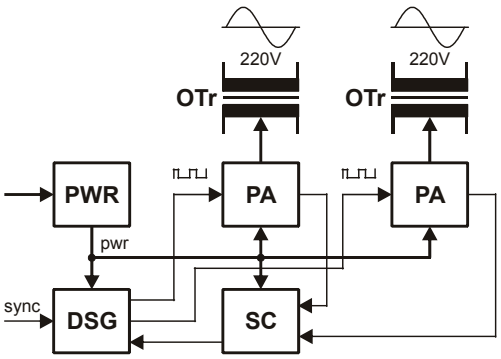

Fig 3. Block diagram of signal supply with new digital signal generator

It is anticipated that the new digital signal generator module will use the pulse width modulation (PWM) to generate sine wave signal.

3 Digital signal generator

There exists several ways to synthesize a digital sinusoid. For example, the coordinate rotation digital computer (CORDIC) algorithm, by which we can determine the sine values by series of micro rotations. Another method is to accumulate phase increments and then use the accumulated phase value to address a look-up table (LUT) that contains precomputed sinusoid values (waveform). These principles are generally called numerically controlled oscillators (NCO) or direct digital frequency synthesizers (DDFS or DDS) [1, 2].

The developed digital signal generator use direct digital frequency synthesis. The block diagram of realized DDS logic is shown in Figure 4.

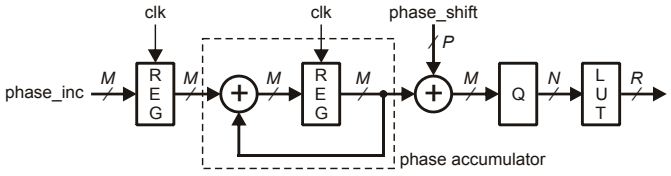

Fig 4. DDS logic block diagram

The DDS block consists of a phase increment register, an adder and a register which form the phase accumulator, phase shift adder, quantizer (*Q*) and look-up table (phase to waveform converter).

The sine wave sequence generated by the direct digital frequency synthesizer is defined by the following equation:

$$x[nT] = A\sin(2\pi f_0 nT + \varphi) \tag{2}$$

Where T is clock period ($T = 1/f_{clk}$), A is equal to 2^{R-1} (R is a magnitude resolution), f_0 is the output frequency which is based on a phase increment value ϕ_{inc} (see Equation 3) and φ is a phase shift which is given from the phase shift value ϕ_{ps} (input *phase_shift* in Figure 4) by the Equation 4.

$$f_o = \frac{\phi_{inc} f_{clk}}{2^M} \tag{3}$$

Where ϕ_{inc} is the phase increment value (input *phase_inc* in Figure 4), f_{clk} is the clock frequency and M is resolution of the phase accumulator.

$$\varphi = \frac{\phi_{ps}}{2^P} \tag{4}$$

Where ϕ_{ps} is the phase shift value (input *phase_shift* in block diagram), and P is the phase shift input resolution.

The frequency resolution of the digital signal generator f_{res} is given by the equation:

$$f_{res} = \frac{f_{clk}}{2^M} \quad (5)$$

This frequency is also the minimum possible output frequency of the digital signal generator. The frequency is generated for the case where in the Equation 3 ϕ_{inc} is equal to 1.

At the end of the DDS logic (Figure 4) two quantizers are included. The phase quantizer (Q) is first and the amplitude quantizer (LUT) is second. The phase qunatizer is a simple slicer that helps us to reduce a number of memory words of the look-up table. This phase quantization introduces a phase noise, which produces unwanted spurious spectral components (called spurs) in the DDS output signals [2, 3]. The difference between the output frequency f_0 (carrier level 0 dB) and the maximum level of spurs is called spurious free dynamic range (SFDR), which is defined by equation:

$$S_{MAX} = -SFDR = -6.02N + 3.992 \quad [dB] \quad (6)$$

The look-up table quantizes the output of the DDS signal to R bits (word length of the output amplitude, i.e. memory word width). This quantization results in a noise to signal ratio which can by approximated by equation:

$$NSR = -SNR = -6.02R - 1.761 \quad [dB] \quad (7)$$

It is important to obey the condition: $S_{MAX} < NSR$. The compliance of this condition will guarantee that the unwanted signal components are caused by the amplitude quantization and not by the phase truncation. The following condition is derived:

$$N > R + 0.956 \quad (8)$$

The required memory size for storing full waveform is given by equation:

$$MS = 2^N * R \quad [bits] \quad (9)$$

Several ways exist how to reduce required memory size for higher values of N and R (for example store only quarter of sine wave or use sine wave approximation).

3.1 Realization

The pulse width modulation clock frequency f_{pwm} = 6 MHz and 8 bit resolution in magnitude was selected for a realization, having regard to the parameters of the power amplifier (PA). These parameters determine the clock frequency f_{clk} and bit widths of the direct digital frequency synthesizer.

The clock frequency f_{clk} is then given by the equation:

$$f_{clk} = \frac{f_{pwm}}{2^R} = \frac{6 \cdot 10^6}{2^8} = 23437.5 \quad [\text{Hz}] \quad (10)$$

These bit widths of the DDS module were chosen as follows R = 8, N = 10, P = 10 and M = 24.

From the Equation 5 we have computed the frequency resolution f_{res} = 0.001397 Hz of the signal generator. From the Equation 6 we obtained S_{MAX} = −56.208 dB, from the Equation 7 we obtained NSR = −49.921 dB and finally from the Equation 9 we got required memory size MS = 8192 bits.

3.2 Realization in VHDL

The digital signal generator was written in VHDL language. The system consists of several modules. The block diagram of the realized system in the FPGA device is shown in Figure 5.

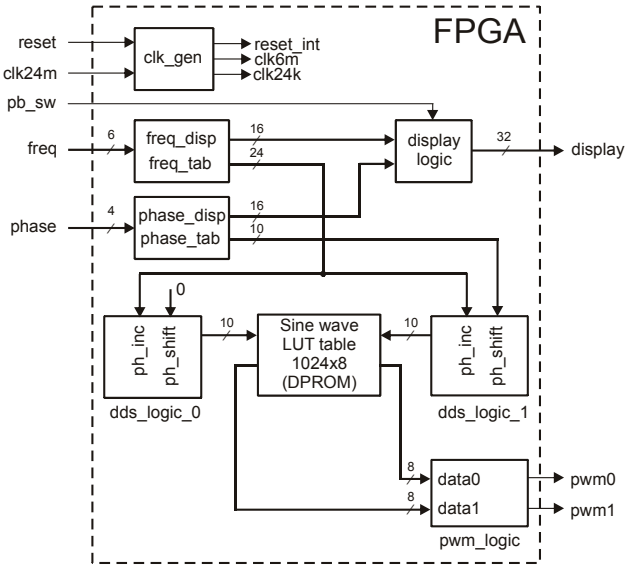

Fig 5. Block diagram of realized signal generator

The generator consists of a clock generator which generates clock signal 6 MHz for PWM module from input clock (24 MHz) and 23.4375 kHz for DDS module. Next there are blocks which compute for selected output frequency and phase shift appropriate phase increment value and phase shift value.

The realized DDS logic module is fully parameterizable, i.e. the accumulator precision (M), the phase shift precision (P) and the phase shift quantizer precision (N) can be set. The amplitude quantizer (LUT) is not included in the DDS module, because the realization is easy to change (full, quarter, sine wave

approximation, etc). The parameters $R = 8$ and $N = 10$ are relatively small so we decide to realize the amplitude quantizer by a full waveform LUT. The generator includes two DDS generators, so two amplitude quantizers are needed. The simple trick was used to realize the LUT table as a dual port ROM. Two amplitude quantizers use only one 8 kbit memory block.
The generator includes block which displays the generated frequency and phase shift on 4 digit seven segment display. The switching between the displayed frequency and phase shift is done by push button (*pb_sw*). Finally there is block for generation of PWM output signals. The depth of the PWM modulation is limited from 5.25% to 94.75% by an appropriate content of LUT memory (amplitude quantizer).

4 Verification and measurements

The testbench was written in the VHDL language for the designed digital system and the design was successfully verified in VHDL simulator by the functional simulation. Finally the design was synthesized to the FPGA device EP1C3T144C8 and successfully verified by timing simulation. The design contains 237 LE (Logic elements), 115 flip-flops and 8 kbits of embedded memory.

Figures 6 and 7 shows measured frequency spectrums of 75.0 Hz and 275.0 Hz output signals of the realized digital signal generator. The frequency spectrum was measured at the output of the amplitude quantizer (look-up table) after D/A conversion by FFT dynamic signal analyzer Agilent 35670A. The spectrum was measured in the range 0 to 800 Hz which is important for the railway signalling technology. Measured spectrum of the 75.0 Hz output signal (Figure 6) shows that maximum level of unwanted signals is better than −66 dBc.

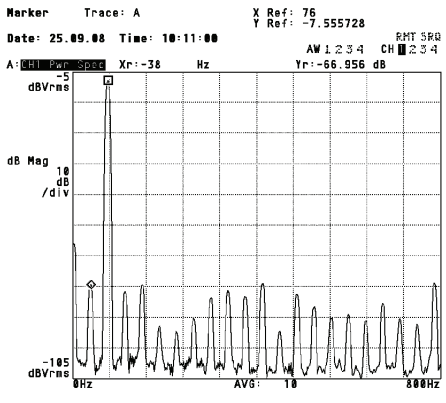

Fig 6. Spectrum of output signal 75.0 Hz

The measured spectrum of the 275.0 Hz output signal (Figure 7) shows that maximum level of unwanted signals is better than −60 dBc.

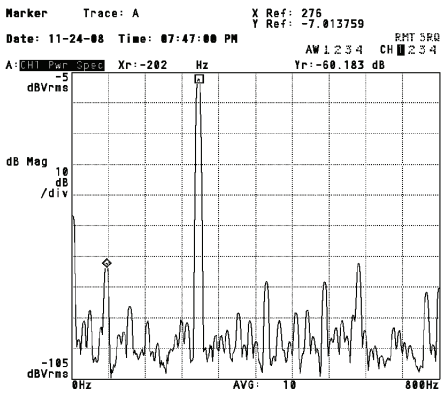

Fig 7. Spectrum of output signal 275.0 Hz

5 Conclusion

The main goal of the design was to develop and verify new digital signal generator for the railway signalling technology. This goal was satisfied and fully functional digital signal generator was developed. The generator is able to generate the output signals in the range of 74 to 76 Hz and 274 to 276 Hz with 0.1 Hz step with phase shit from 0 to 180 degrees with 15 degrees step. The digital signal generator was realized on printed circuit board size 165x100 mm (small EURO card). The generator was successfully verified by measurement on FFT dynamic signal analyzer. The signal generator due to use of the direct digital frequency synthesis generates the sine wave output signals with very low distortion of the signal.

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