Electronic Replacement of Electro-Mechanic Phase Sensitive Relay

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***Abstract* – This article deals with the design of a digital signal processing system in a programmable logic device. The system is being developed for using as a high safe replacement of an electro mechanic phase sensitive relay type DSŠ-12. These relays are used by the Czech Railways for detecting the presence of railway vehicles at the rail circuit. For digital signal processing was used discrete Fourier transform, iterative algorithm CORDIC and thresholding.**

I. INTRODUCTION

At present time electro-mechanic relays are used as a railway signaling technique by the Czech Railways. These relays are used for detecting the presence of railway vehicles at the rail circuit. The rail circuit is shown in Fig. 1. The rail circuit consists of an isolated rail segment, transformers, source of signaling frequency and the phase sensitive relay type DSŠ-12.

The signal supply generates a 75 Hz (or 275 Hz) sinusoidal signal. The signal supply has two outputs phase shifted by 90 degrees. The presence of the railway vehicle in the rail segment can be detected by changes in amplitude and phase on the rail signal against the reference signal. The change in amplitude or in phase or in both must be signalled by the relay. The DSŠ-12 relays are hence sensitive in amplitude and phase (relays are working on the principle known as Ferraris motor). The replacement of electro-mechanical phase sensitive relay leads to the design of a special digital signal processing (DSP) system. The input signals must be converted from analogue to digital representation by A/D converters and further processed by digital signal processing methods.

II. DIGITAL SIGNAL PROCESSING ALGORITHM

Because we want to implement the whole DSP system in one programmable logic device (PLD), we must select suitable algorithms specific to this architecture. As stated above it is evident that the algorithm must compare amplitude and phase of two signals.

Amplitude and phase of digitalised signal can be computed with the aid of discrete Fourier transform (DFT) [1], [2].

$$X_k = \sum_{i=0}^{N-1} x_i e^{-j(2\pi/N)ik} = \sum_{i=0}^{N-1} x_i W_N^{ik}, \quad k = 0,1,...,N-1 \qquad (1)$$

As the result of the one point DFT computation at frequency 75 Hz (or 275 Hz) for rail and reference digitalized signals, we get two complex vectors. For each complex vector we can compute its amplitude and phase:

$$M = |X_k| = \sqrt{x_{k\,re}{}^2 + x_{k\,im}{}^2}, \quad \varphi = \tan^{-1}\left(\frac{x_{k\,im}}{x_{k\,re}}\right) \qquad (2)$$

The realization of square root and $\tan^{-1}$ functions in PLD device is fairly complex. Computation of amplitude and phase of a given complex vector can be done by an iterative algorithm, e.g. CORDIC (COrdinate Rotation DIgital Computer) algorithm [3], [4]. This algorithm works on the principle of vector rotation in plane by a series of micro rotations. The one micro rotation is defined as:

$$\begin{aligned} x[j+1] &= x[j] - \sigma_j 2^{-j} y[j] \\ y[j+1] &= x[j] + \sigma_j 2^{-j} y[j] \\ z[j+1] &= z[j] - \sigma_j \tan^{-1}\left(2^{-j}\right), \quad \text{where } \sigma_j \in \{-1,1\}. \end{aligned} \qquad (3)$$

Where x is real part, y is imaginary part of the vector and z is accumulated angle. Only three additions / subtractions, two shift operations and one pre-computed table with angles are required for the implementation of one micro rotation. The CORDIC algorithm multiplies the vector amplitude by factor K ≈ 1.64676.

The computed amplitude of the rail signal has to be compared to the preset thresholds. The two threshold values define the hysteresis. Next we need to compute the difference between the phases of the two vectors, and to compare the difference with a preset range, again with hysteresis. These two outputs logically ANDed indicate whether the rail segment is free or occupied by a railway vehicle.

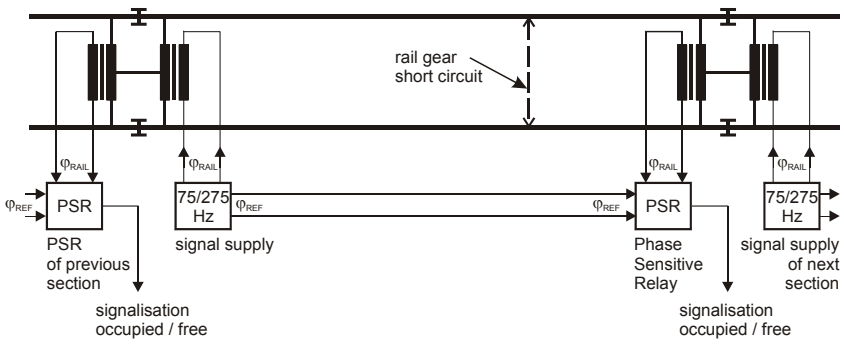

Fig. 1. Rail circuit

III. DESIGN OF DSP ALGORITHM

To verify the suggested digital signal processing algorithm, an experimental model of the electronic phase sensitive relay [5] was built. The model consists of the analog-digital hardware module and the software program (written in C language) that runs on a PC platform. The analog part of module contains the over-voltage protection, an operational amplifiers network for the adjustment of input voltage range, successive approximation 16-bit A/D converters with serial output, 2.5V voltage reference and 10 Mbps optocouplers for the galvanic isolation between the analog and the digital part. The digital part of module consists of a PLD device type FPGA (Field Programmable Gate Array) and only samples analog signals and transfers the digitized samples to a PC through the parallel port. The analog-digital module allows simultaneous sampling of two analog channels at a sample rate of up to 100 kHz with a 16-bit resolution.

IV. FPGA IMPLEMANTATION

After successful verification of the DSP algorithm on a PC, the whole system was written in VHDL language [6]. The system consists of several modules. First part of system is shown on Fig. 2. There are a clock generator that generates 2.4 MHz clock for the A/D converters and 3.6 kHz clock for sampling, and a module that controls data acquisition with serial A/D converters. The next blocks are ROMs with sin and cos coefficients for the computation of one point DFT. The Kaiser window with $\beta = 2$ was applied to the coefficients in order to suppress the influence of the buffers boundaries. The buffers are circular with the length of 720 samples.

The samples from ADC block are shifted to the circular buffers. A one point DFT is then computed over each buffer. Block of one point DFT computation is shown on top of Fig. 3. With the sample rate 3.6 kHz and the length of a 720-sample buffer, the frequency resolution is 5 Hz per point. Complex 18-bits wide vectors are obtained for each buffer after the computation of one point DFT. The amplitude and phase is then computed by 13 iterations of CORDIC algorithm for each vector. CORDIC block is shown on bottom of Fig. 3.

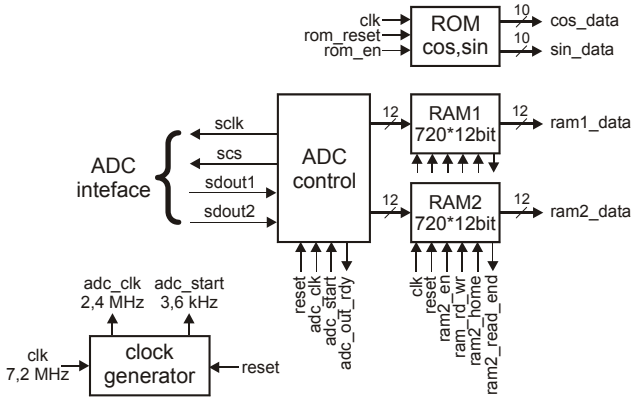

Fig. 2. Clock generator, ADC control, RAM buffers and ROMs with coefficients

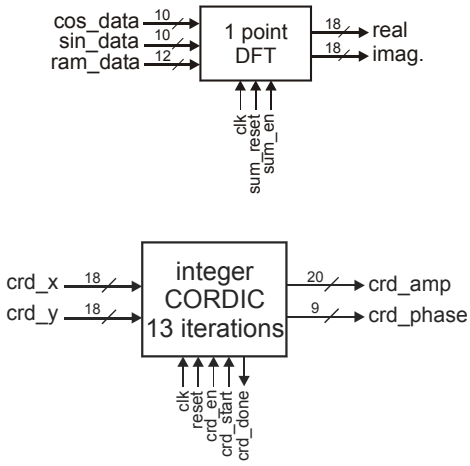

Fig. 3. One point DFT block (top) and CORDIC block (bottom)

The 20-bit width amplitude and 9-bit width phase are obtained after 13 iterations of CORDIC algorithm. After this rectangular to polar conversion, the algorithm continues by the comparison of threshold and computed values of amplitude and phase with hysteresis. A final output of this threshold logic is then computed by an AND logic function. This block is shown on left side of Fig. 4.

A programmable pull time and drop time of the relay is required. A simple circuit implements this output-signal timing. The output of the threshold logic controls two counters – "False" counter and "True" counter. The "False" counter counts up when the output of the threshold logic is log. 0, and counts down when the output of the threshold logic is log. 1. The "True" counter counts vice versa. The counters count up to a specified values and do not overflow or underflow. The output of the relay is log. 0 when the "False" counter reaches a specified value and log. 1 when the "True" counter reaches the other specified value. Block that realizes output-signal timing is shown on right side of Fig. 4. This output-signal timing logic allows set the pull time of the relay in range between 140 ms and 10 s. The drop time is fixed set to 100 ms.

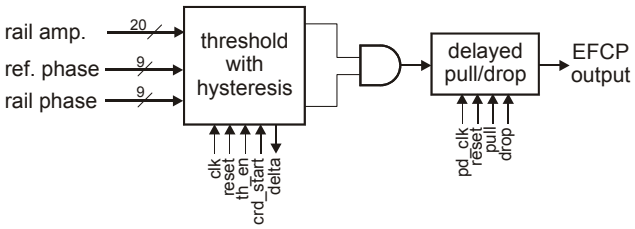

Fig. 4. Threshold block and programmable pull / drop time block

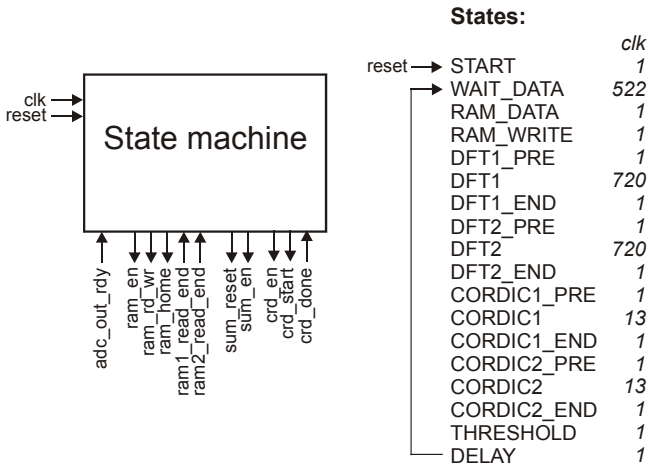

Fig. 5. Finite state machine

All mentioned blocks are controlled by a finite state machine. This finite state machine controls the write cycles to the registers and sets the control signals. The state machine runs at a clock frequency of 7.2 MHz. Function of finite state machine is shown on Fig. 5.

The whole system was written in VHDL language and successfully simulated in ModelSim. Input data from serial A/D converters was read from binary files stored on disk. The first realization was done using Altera's Quartus II system on development kit (shown on Fig. 6). The realized circuit contains over 1700 LUTs (Look-Up Tables), 500 flip-flops and 5.5 kB RAM memory. The computational power of the realized system is 21 MOPS (Million Operations Per Second) at clock frequency of 7.2 MHz. At the present time is under development prototype sample on Euro card with Cyclone EP1C6 device.

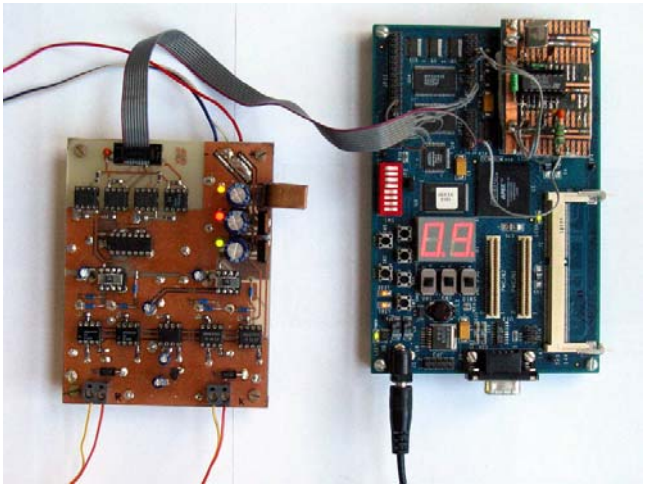

Fig. 6. Functional prototype

V. CONCLUSION

The main goal of the design was to create algorithms for the electronic version of a phase sensitive relay. This goal was reached and fully functional concept prototype was successfully developed. Due to the use of digital signal processing the electronic version of the relay has better parameters than the electro-mechanical relay. The whole system consists of only an oscillator, one FPGA device, and an analog module for A/D conversion. This type of a digital system implementation is called "System On Programmable Chip" (SOPC). This system achieves excellent performance and reliability through the use of low number of devices.

VI. ACKNOWLEDGMENT

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