Electronic phase sensitive receiver for railway signalling technology

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Abstract: This article deals with a design of a replacement of an electro mechanic phase sensitive relay type DSS-12. These relays are used by the Czech Railways for detecting the presence of railway vehicles at the rail circuit. The replacement of electro-mechanical phase sensitive relay leads to the design of a special digital signal processing (DSP) system. The input signals must be converted from an analogue signal to a digital representation by A/D converters and further processed by digital signal processing methods. Discrete Fourier transform, an iterative algorithm CORDIC and threshold was used for digital signal processing. The digital signal processing system was implemented in C language and then rewritten to the VHDL language to implement it in the FPGA (Field Programmable Gate Array) device.

Key-Words: phase sensitive relay, DSS-12, railway signalling technology, rail circuit

1 Introduction

At present time electro-mechanic relays are used as a railway signalling technology by the Czech Railways. These relays were developed in the 1960 and are used for detecting the presence of railway vehicles at the rail circuit.

2 Railway circuit

The railway circuit is shown in Figure 1. The railway circuit consists of an isolated rail segment, transformers, source of signalling frequency and the phase sensitive relay type DSS-12.

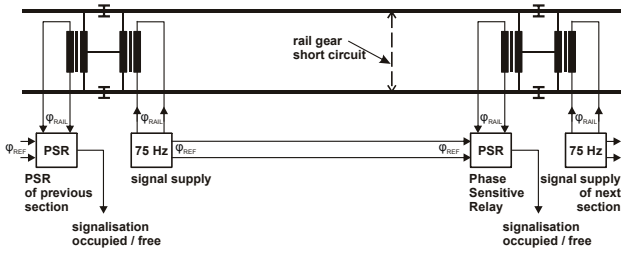

Fig. 1 Railway circuit

The railway circuit is electrical circuit with spread parameters. Thus when the moving rail gear makes a short circuit between rails then both an amplitude and phase of the rail signal will change in time.

The source of the signalling frequency generates the 75 Hz or 275 Hz sinusoidal signal. The source of the signalling frequency has two outputs phase shifted by 90 degrees. One of the outputs is connected through the transformer to the rail circuit. The second output is connected to the reference input of the phase sensitive relay. At the opposite end of the railway circuit is signal from the second transformer connected to the second input of the phase sensitive relay. The presence of the railway vehicle in the railway segment can be detected by changes in the amplitude and phase of the rail signal against the reference signal. The change of both the amplitude and phase is detected by the relay. The phase sensitive relay is hence sensitive in the amplitude and phase.

2.1 Phase sensitive relay DSS-12

The phase sensitive relay DSS-12 (shown in Figure 2) is working on the principle well known as Ferraris motor.

Fig. 2 Phase sensitive relay DSS-12

The phase sensitive relay consists of two coils turned over 90 degrees. An aluminium plate is inserted between them and by a torque M acts on contacts. The torque M is proportional to the product of currents in coils and

function *sin* φ (Equation 1). Where the φ is phase angle between currents I_1 and I_2.

(1) $M = k\, I_1\, I_2 \sin\varphi$

The maximum moment happens when the phase angle φ is equal to 90°. The output of the relay changes if deviation of the plate exceeds some level.

Because these relays are present at the each segment of the railway (length 100 m to 1.5 km) and they have an expensive maintenance a new design of their electronic version is being developed.

3 Digital signal processing algorithm

The digital signal processing algorithm was developed. The algorithm does computation analogous to the phase sensitive electro-mechanical relay DSS-12 (follow the Equation 1) and was designed with respect to easy implementation in the FPGA (Field Programmable Gate Array) device. At the beginning the signals (railway and reference) are converted from the analogue signal to digital representation by A/D converters.

3.1 Computation of amplitude and phase

The amplitude and phase of the digitalized signal can be computed by discrete Fourier transform (DFT) [1, 2].

(2) $$X_k = \sum_{i=0}^{N-1} x_i e^{-j(2\pi/N)ik} = \sum_{i=0}^{N-1} x_i W_N^{ik}, \quad k = 0,1,\ldots, N-1$$

As the result of the one point DFT computation at frequency 75 Hz or 275 Hz for the railway and reference digitalized signals, we get two complex vectors. For each complex vector we can compute its amplitude and phase by

(3) $$A = |X_k| = \sqrt{{x_{k\,re}}^2 + {x_{k\,im}}^2}, \quad \varphi = \tan^{-1}\left(\frac{x_{k\,im}}{x_{k\,re}}\right)$$

The direct realization of square root and $\tan^{-1}$ functions in the FPGA device is fairly complex and inefficient. Computation of the amplitude and phase of a given complex vector can be done by an iterative algorithm, e.g. CORDIC (COrdinate Rotation DIgital Computer) algorithm [3, 4]. This algorithm works on the principle of vector rotation in a plane by a series of micro rotations. The one micro rotation is defined as:

(4) $$\begin{aligned} x[j+1] &= x[j] - \sigma_j 2^{-j} y[j] \\ y[j+1] &= x[j] + \sigma_j 2^{-j} y[j] \\ z[j+1] &= z[j] - \sigma_j \tan^{-1}\left(2^{-j}\right), \quad \text{where } \sigma_j \in \{-1,1\}. \end{aligned}$$

Only three additions / subtractions, two shift operations and one pre-computed table with angles are required for the implementation of one micro rotation.

For a computation of the amplitude and phase of the vector we assign in Equation 4 to x real part and to y imaginary part of the vector. After several micro rotations we obtain in z accumulated angle (initial value is 0). The CORDIC algorithm multiplies the vector amplitude by a factor $K \approx 1.64676$.

3.2 Computation of torque *M*

For the computation of the torque M we need to compute trigonometric function *sin* of the phase angle φ (phase difference of the vectors). This computation also can be done through the CORDIC algorithm. At the beginning of the computation we assign $x = 1$, $y = 0$ and $z = \varphi$. We obtain after several micro rotations in x result of the function *cos* φ and in y result of the function *sin* φ. Now we have computed out all variables (I_1, I_2 and *sin* φ) and we can compute the torque M by the multiplication of them. For the multiplication we can use hardware multipliers which are commonly available in today's FPGA devices.

The computed torque M has to be compared to the preset thresholds. The two threshold values define the hysteresis. The output of the comparator is logical signal which indicates whether the railway segment is free or occupied by a railway vehicle.

3.3 Delayed output

The electro-mechanic phase sensitive relay has some reaction time (pull time and drop time). This output signal timing must be realized even in the DSP algorithm. The programmable pull time and drop time was realized by a simple circuit.

The output of the threshold logic controls two counters – "False" counter and "True" counter. The "False" counter counts up when the output of the threshold logic is logical 0, and counts down when the output of the threshold logic is logical 1. The "True" counter counts vice versa. The counters count up to specified values and do not overflow or underflow. The output of the relay is logical 0 when the "False" counter reaches a specified value and logical 1 when the "True" counter reaches the other specified value.

3.4 Verification of DSP algorithm

An model of the electronic phase sensitive relay [5] was built to verify the suggested digital signal processing algorithm. The model consists of the analogue-digital hardware module and the software part (program) that runs on a PC platform.

The analogue part of the module contains the over-voltage protection, an operational amplifiers network for the adjustment of the input voltage range, successive

approximation 16-bit A/D converters with serial output, 2.5V voltage reference and 10 Mbps optocouplers for the galvanic isolation between the analogue and the digital part of the circuitry. The digital part of module consists of a FPGA device only and samples analogue signals and transfers the digitized samples to a PC through the parallel port. The analogue-digital module allows simultaneous sampling of two analogue channels at a sample rate of up to 100 kHz with a 16-bit resolution.

The software part was written in C language. It supports three simulation input data modes. First two modes do offline simulation with an interactively generated data or with a data stored in binary files. The third mode supports real-time simulation with the data acquisition from the hardware module (real data).

3.5 Implementation in the FPGA device

After the successful verification of the DSP algorithm on a PC, the whole system was rewritten into VHDL language. The system consists of several modules. Block diagram of the realized system in the FPGA device is shown in Figure 3.

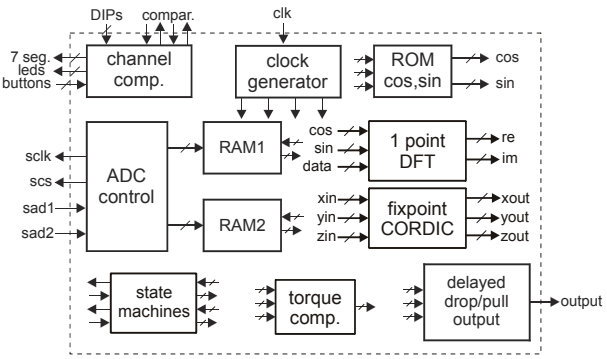

Fig. 3 Block diagram

A clock generator generates sample clock and master clock for serial A/D converters and clocks for finite state machines. ADC control module controls data acquisition with serial A/D converters. The next blocks are ROMs with sin and cos coefficients for the computation of one point DFT. The Kaiser window with $\beta = 2$ was applied to the coefficients in order to suppress the influence of the buffers boundaries. The samples from ADC block are shifted to the sample buffers. A one point DFT is then computed over each buffer. The frequency resolution of the realized DFT is 5 Hz per point. The complex vectors are obtained for each buffer. The amplitude and phase of the vectors is then computed by the iterative CORDIC algorithm. After the rectangular to polar conversion, the algorithm continues to compute function sin of the phase difference again by the CORDIC algorithm. Finally the torque is computed by two multiplications, the threshold function is performed and delayed drop/pull output function is realized. All mentioned blocks are controlled by finite state machines.

Because the whole system must be safe, the reciprocal comparison (block channel comp. in Figure 3) was designed. The system consists of two identical channels and these channels compare each other several results of their computations. The amplitudes, phases, torque, final output and several internal states are compared.

The system was written in the VHDL language and successfully simulated in VHDL simulator by functional and finally by timing simulation. The simulated input data for serial A/D converters was read from binary files stored on disk.

4 Conclusion

The main goal of the design was to create and verify digital signal processing algorithm. This goal was satisfied and fully functional model was successfully finished. The system realized in the one FPGA device Altera EP2C8 and contains over 2000 LUTs (Look-Up Tables), 600 flip-flops and 6 kB of embedded RAM memory. The computational power of the realized system is 22 MOPS (fixed point). This type of a digital system implementation is called “System On Programmable Chip” (SOPC). Due to use of the digital signal processing, the electronic version of the relay has advantages. For example in the field of diagnostics of the railway circuit it can monitor the amplitude and phase of the free and occupied railway segment and store these values for diagnostics purposes.

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